Stages in Transistor Fabrication and the Impact of Nanotechnology

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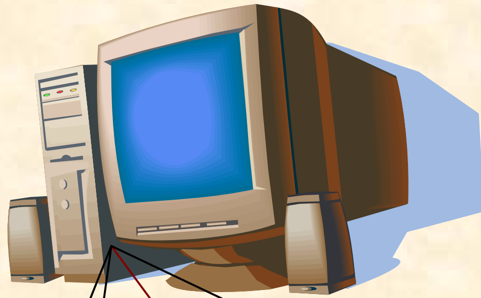
Stages in Transistor Fabrication and the Impact of Nanotechnology

Outlines:

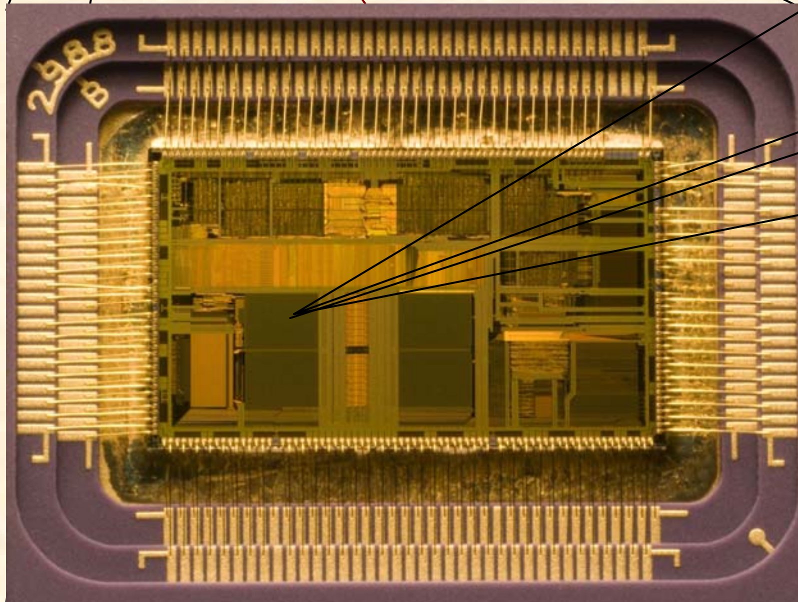
- The MOSFET: The basic unit of a computer microprocesor
- The MOSFET: Scaling down the device
- The MOSFET: How Do We Fabricate them
- The MOSFET: Where Do We Fabricate them
- How Do We See Nanostructures
- Summary: The Impact of the Nanotechnology on the MOSFET

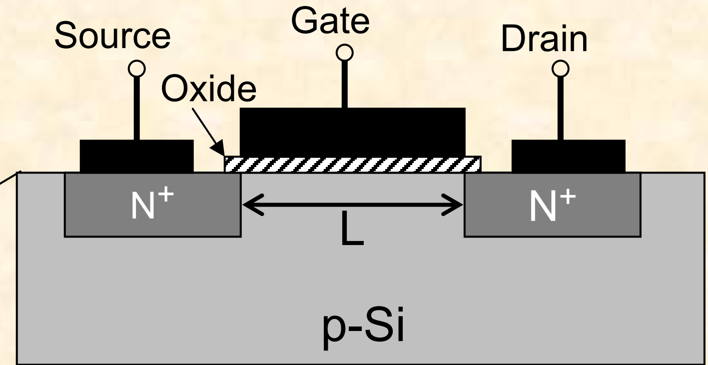
The MOSFET

(Metal-Oxide-Semiconductor Field-Effect Transistor)
A computer microprocessor have billions of MOSFETs



The Microprocessor





Schematic diagram of a MOSFET

$$f = \frac{\mu_n V_D}{2\pi L^2}$$

$$P_{dyn} \sim f\, C_T\, V_{dd}^2$$

Eventually scaling would be limited by power dissipation!!

APPLICATIONS

http://www.techgadgets.in/images/hp-compaq-dc7800-desktop-pc.jpg

http://greenmgpl.files.wordpress.com/2009/02/cellphones.jpg

http://blog.loaz.com/media/blogs/timwang/mini-laptop-fujitsu-P7230.jpg

www.levoltz.com

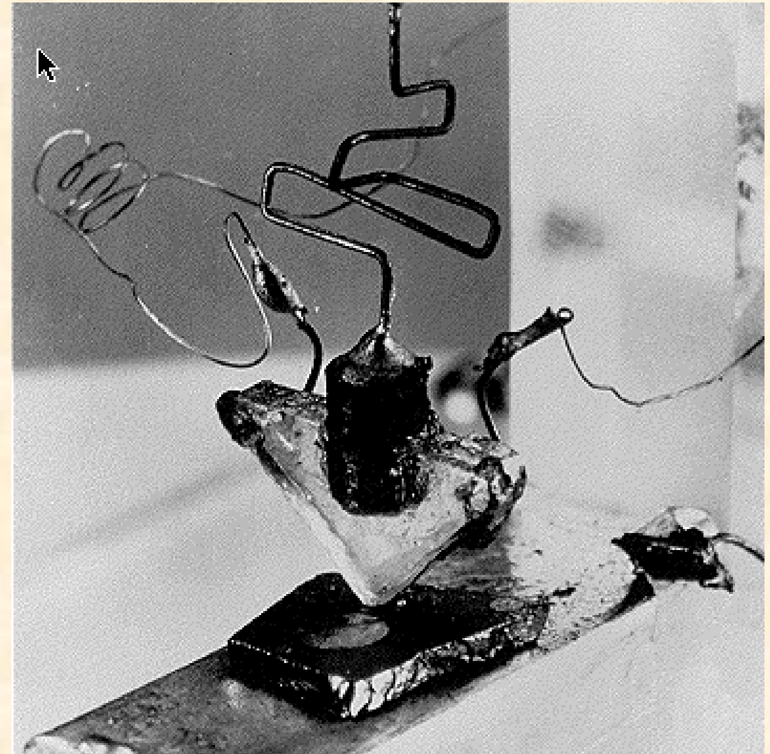
The Giant Early Technologies

1906: Vacuum Tube

1956: Ampex VRX-1000
The First Commercial Videotape Recorder

http://www.cedmagic.com/history/

Giant! Technology

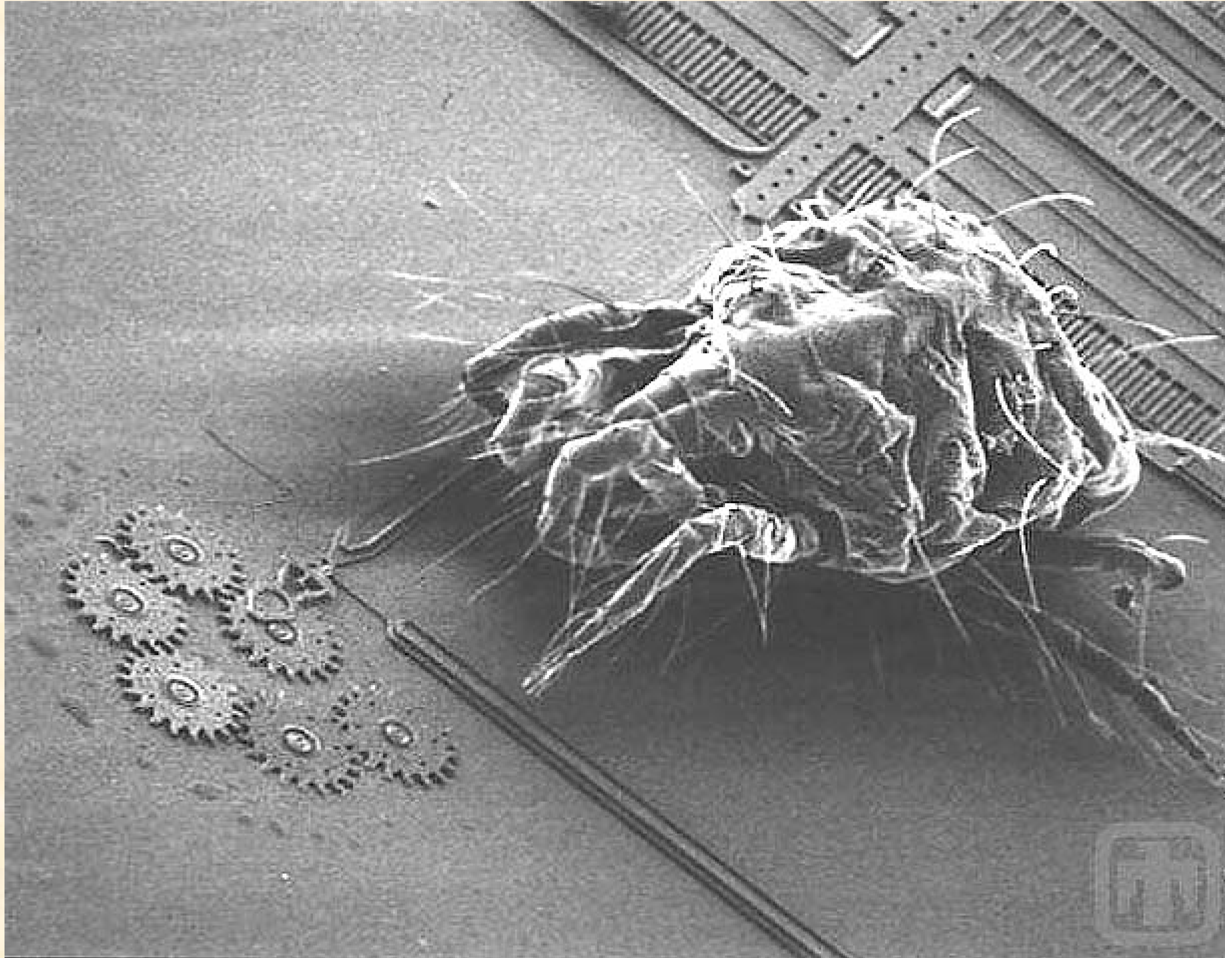


1947: Invention of the Transistor

The first transistor was invented at Bell Laboratories on December 16, 1947 by William Shockley (seated at Brattain's laboratory bench), John Bardeen (left) and Walter Brattain (right).
This was perhaps the most important electronics event of the 20th century, as it later made possible the integrated circuit and microprocessor that are the basis of modern electronics. Prior to the transistor the only alternative to its current regulation and switching functions (TRANSfer resISTOR) was the vacuum tube, which could only be miniaturized to a certain extent, and wasted a lot of energy in the form of heat. Although video was possible with vacuum tube equipment, as was the case with the Ampex VRX-1000, without the transistor video products would never have gotten very small.

http://www.cedmagic.com/history/transistor-1947.html

Scaling



A mite less than 1 mm on a MEMS device.

www.google.com

Shrinking Device Dimensions

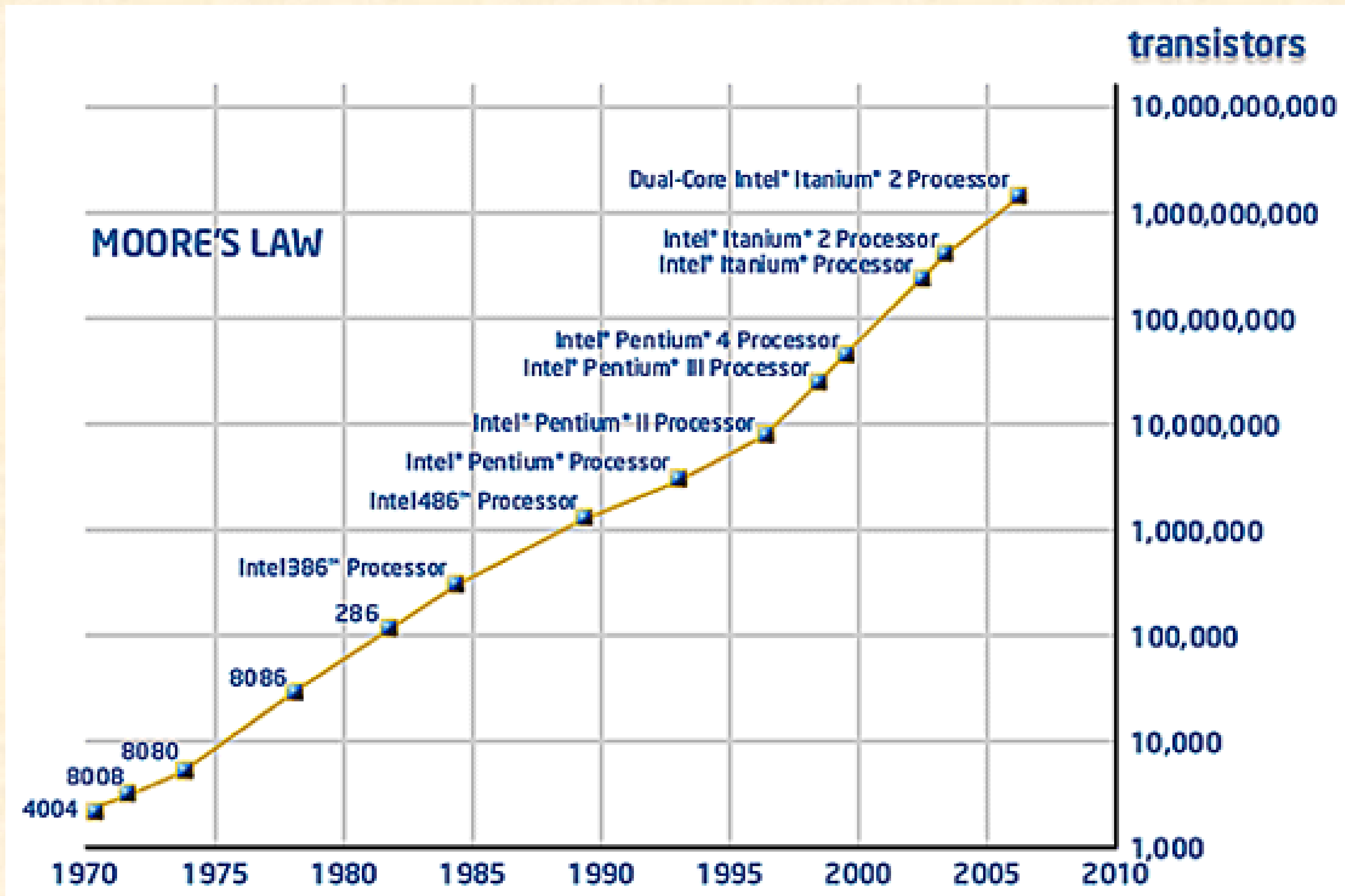
Why do we want to make them small?

Products will be of:

High Density
High Speed
Low Cost
Better Performance

Scaling: *Electronics Keeps On Getting Better*

Moore's "Law": Number of Transistors per Microprocessor Chip



intel.com

Effects of Scaling Down Device Dimensions

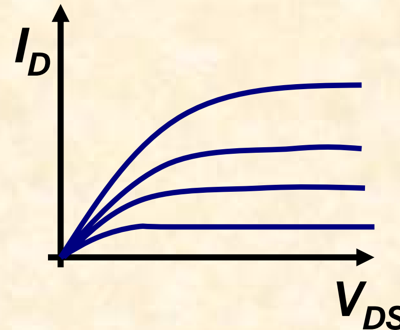
There are rules for scaling!!

- Shrinking L changes the dimensionality of the potential distribution
- **Channel Lenght, L, down from 0.15 µm to 100 nm, to 65 nm, 45 nm, 36 nm, 25 nm, 15 nm...**
  Limited by S/D tunneling
  ➔Change channel material
  ➔To SiGe or Ge!

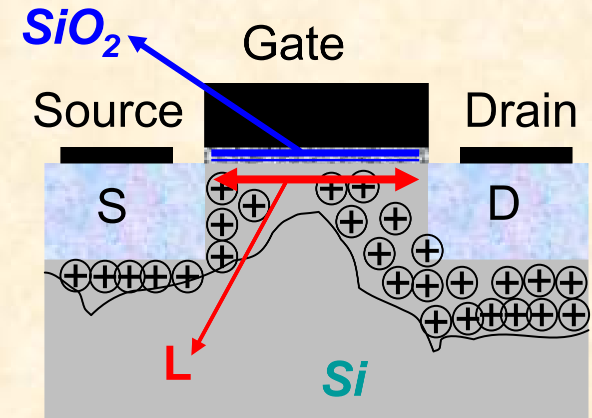
e.g. Carbon Nanotubes

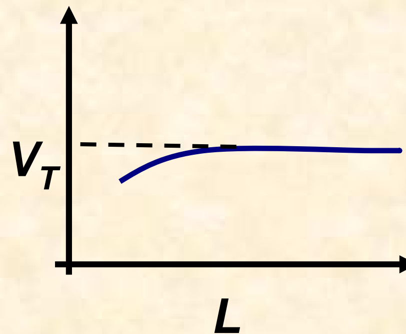
- Thinning Gate Oxide
  Limited by direct tunneling
  ➔Reliability issues
  ➔Change oxide material
  ➔HfO_2, or other high-k oxide

..... Eventually the Si substrate may just be a carrier!!

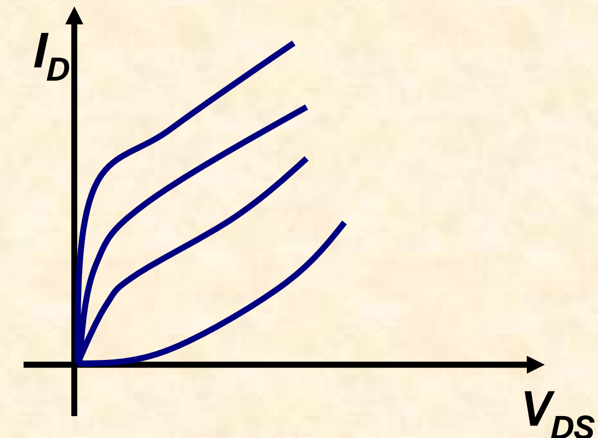


Normal Long Channel characteristics





Effect on Channel length on the threshold voltage



Typical I-V Characteristics of a MOSFET exhibiting Punchthrough effects

M.Y.A. Yousif

Changing the Gate Oxide and the Channel Materials

HfO_2 on strained-Si and strained-SiGe

Layers fabricated using RPCVD at 40 torr and 650 °C

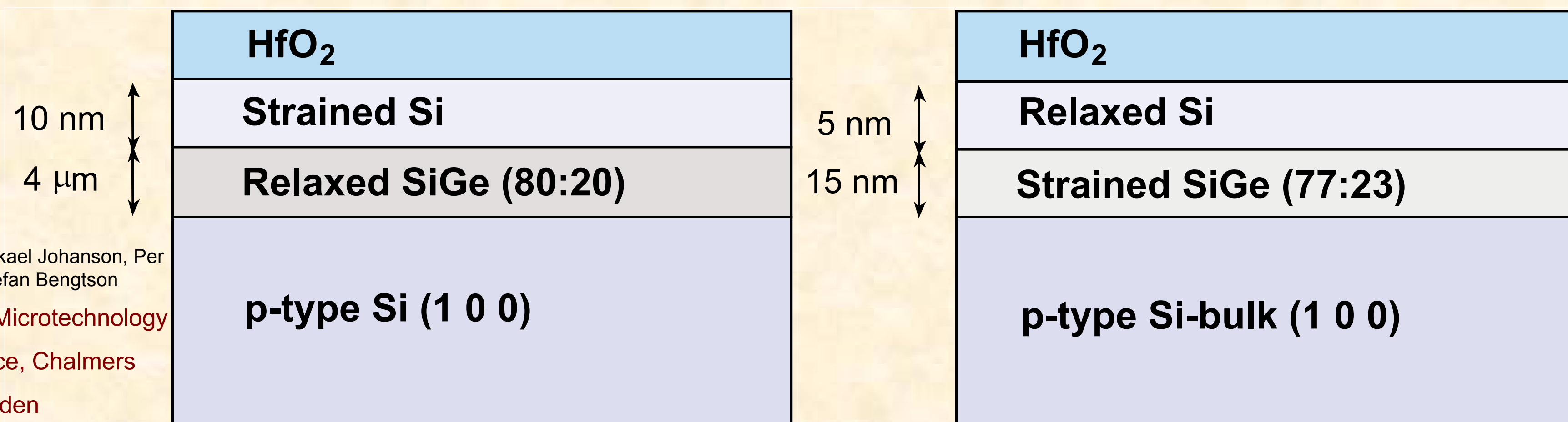
HfO_2 deposited in a hot wall horizontal ALD reactor.

Device description

1. Boron doped p-type Si (1 0 0) wafers ρ = 10 Ω-cm
2. RPCVD performed to grow Strained-Si/Relaxed-SiGe and Strained-SiGe
3. Standard RCA cleaning and HF (2%) dip
4. HfO2 deposition using ALD reactor
5. Standard processing to form Al pads for electrical characterization

Strained Si (StSi)

Strained SiGe (StSiGe)



M.Y.A. Yousif, Mikael Johanson, Per Lundgren and Stefan Bengtson
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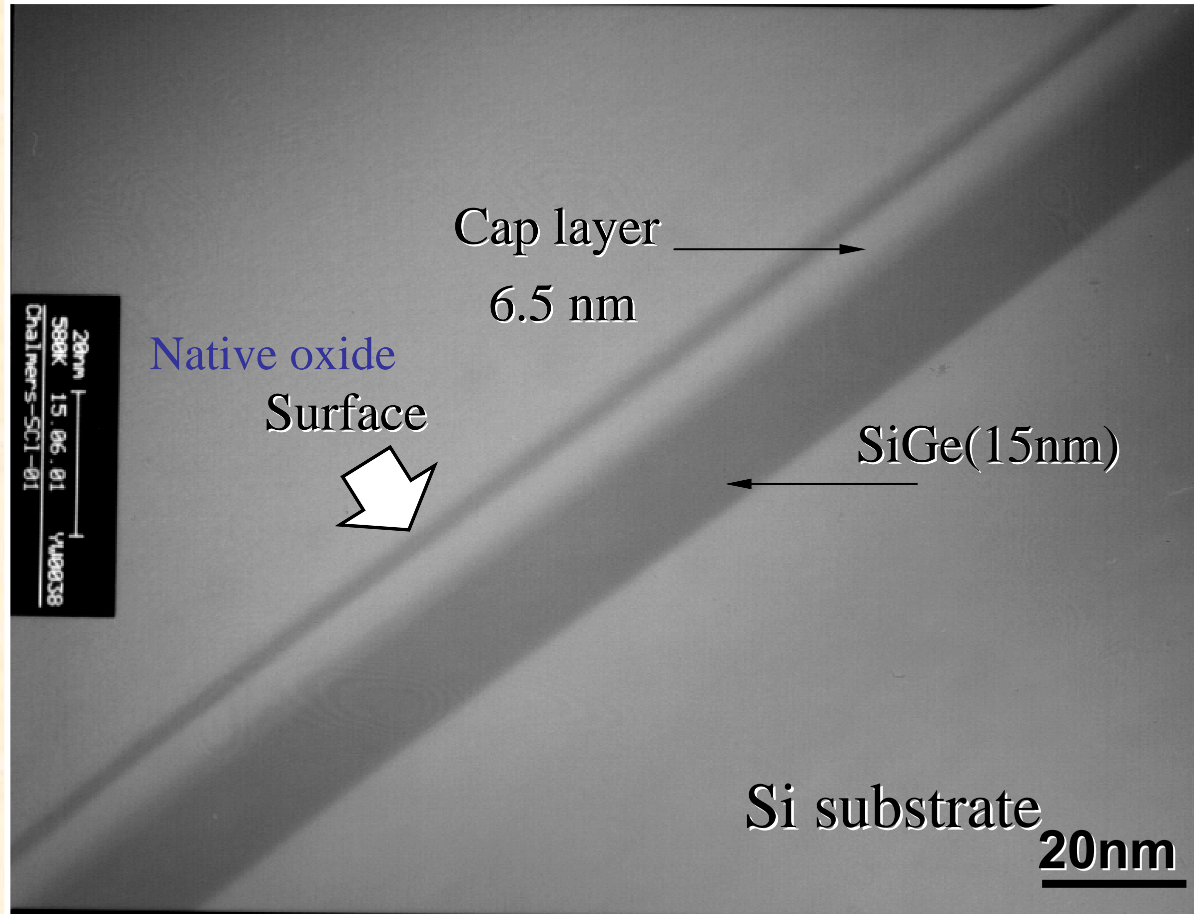
Changing the Channel Material

One SC1 Cycle. Etch~ 2.5 nm



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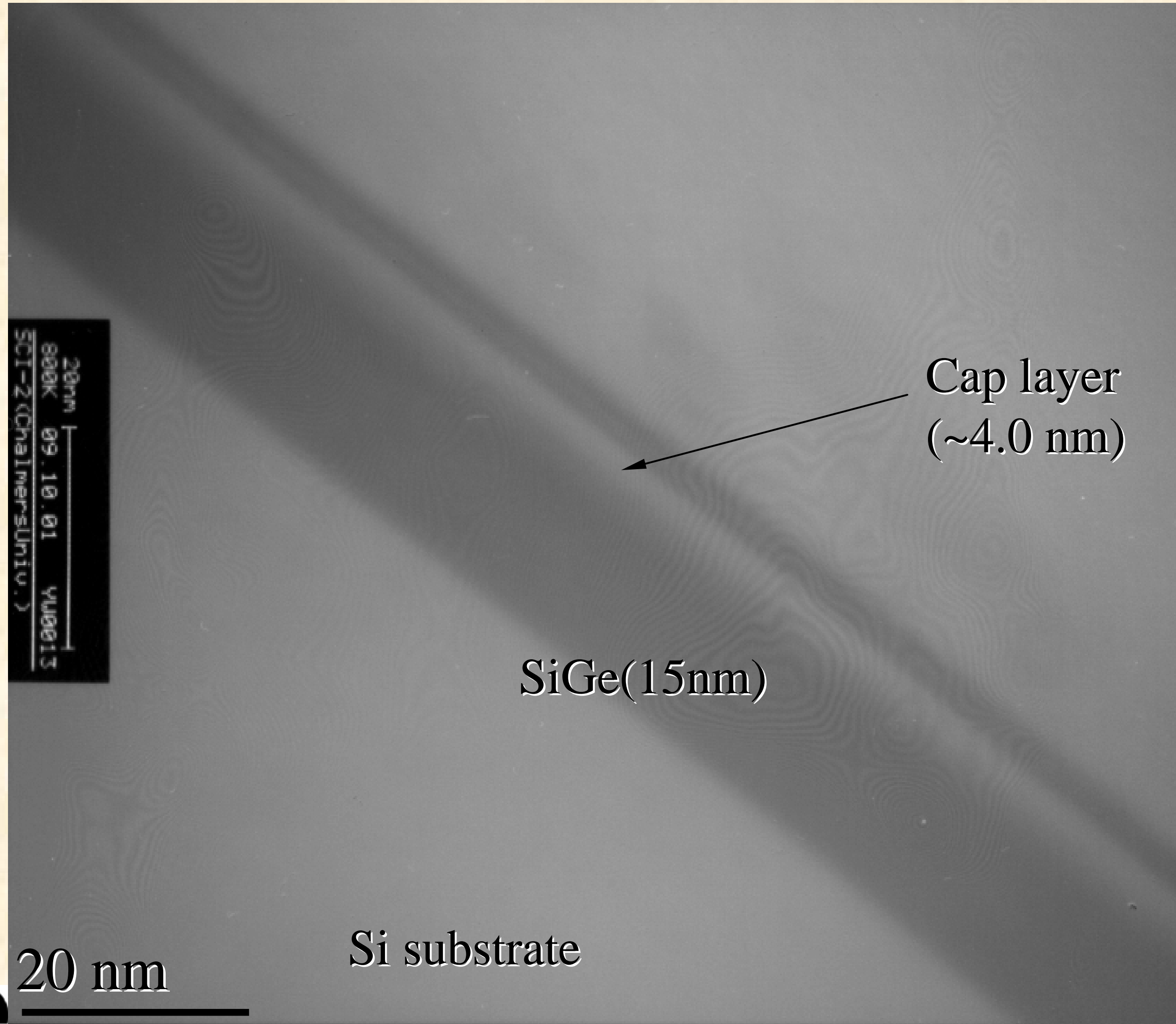
Changing the Channel Material

Two SC1 Cycles. Etch ~5.0 nm



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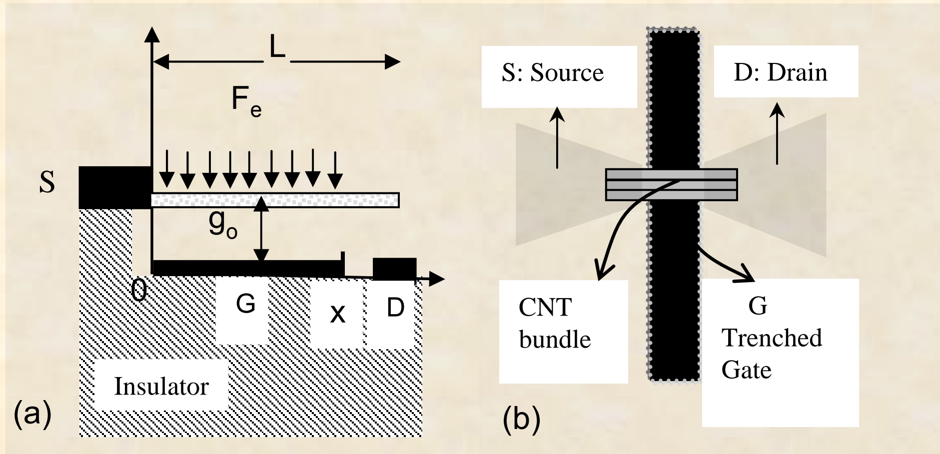
Carbon Nanotubes as a Channel

Nanoelectromechanical Carbon Nanotube-based Switches



$$P_{off} = I_{off} V_{dd}$$

$$I_{off} = \frac{1}{R_o} e^{-y(V)/\lambda} V_{sd}$$

$$P_{dyn} \sim f\, C_T V_{dd}^2$$

LSTP*: low standby power;
LOP*: Low operating power

Year (DRAM ½ pitch)	2011 (40 nm)	2009 (50 nm)	CNT-NEM (estimates, row 4 of Table1, MWNTs)	CNT-NEM (estimates, row 6 of Table1, bundles)
Logic	LSTP*	LOP*		
L_g: Physical gate length (nm)	25	25	25 (1)	25 (1)
Source-drain off-state current (μA/μm)	1.2×10^{-5}	8×10^{-3}	1×10^{-9} (2)	1×10^{-8} (2)
V_{dd}: power supply (V)	1	0.8	0.65 (3)	0.8 (3)
$V_{t,sat}$: saturation threshold voltage (mV)	502	276	428 (4)	542 (4)
$I_{sd,sat}$: Source-drain on-current, $I_{d,sat}$ (μA/μm)	580	652	> 600 (5)	> 1300 (5)
$C_{g,total}$: Total gate capacitance (F/μm)	6.8×10^{-16}	7.37×10^{-16}	3.9×10^{-16} (6)	1.1×10^{-15} (6)
τ: Intrinsic switching delay (ps)	1.17	0.9	74 (7)	48 (7)
1/τ: Intrinsic switching speed (THz)	0.855	1.111	0.013 (8)	0.021 (8)

M.Y.A. Yousif, et. al.,Nanotechnology, **19** (2008) 285204

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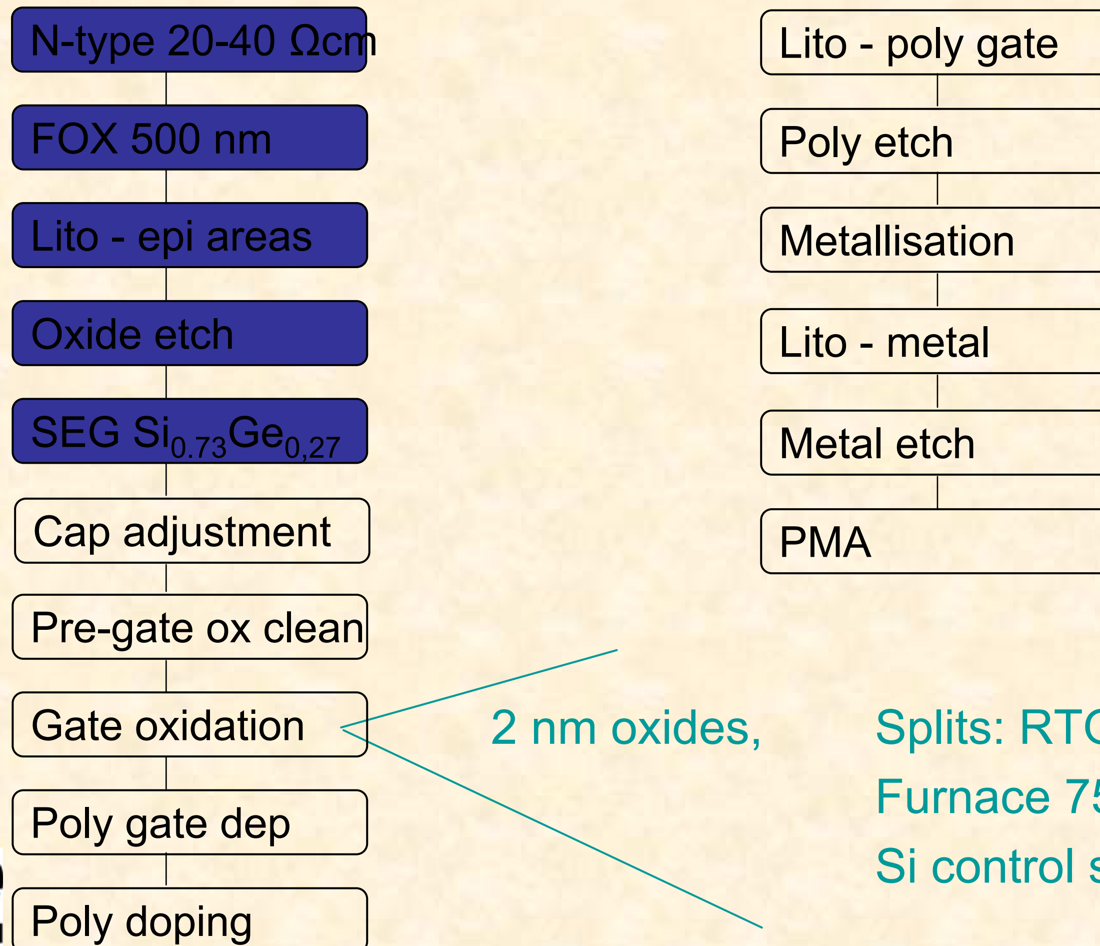
Typical Example of a Process flow



Splits: RTO 850°C, RTO 800°C
Furnace 750°C, Furnace 700°C
Si control samples

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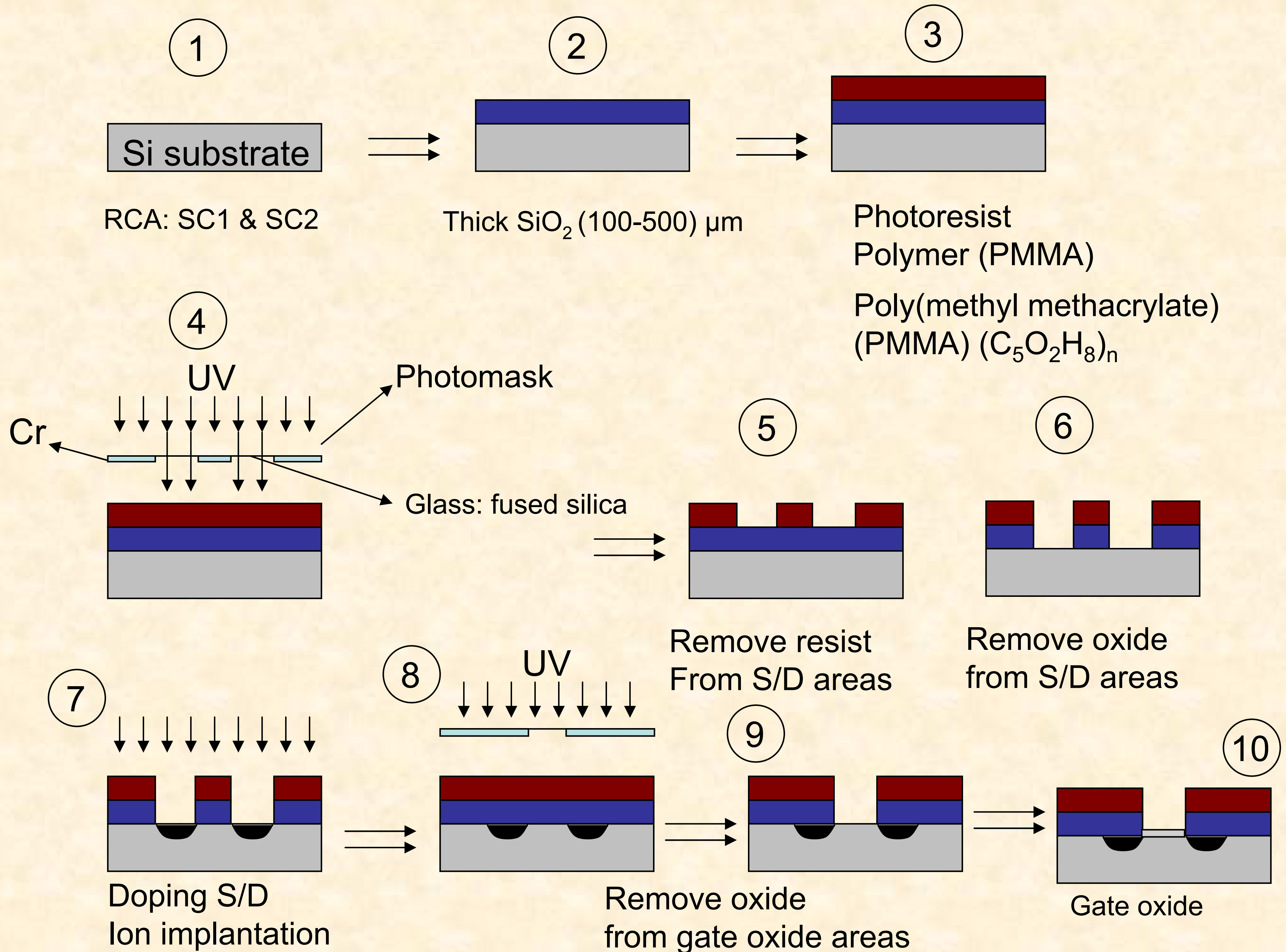
Photolithography

The transferring of geometric patterns on a mask to a surface of a wafer.

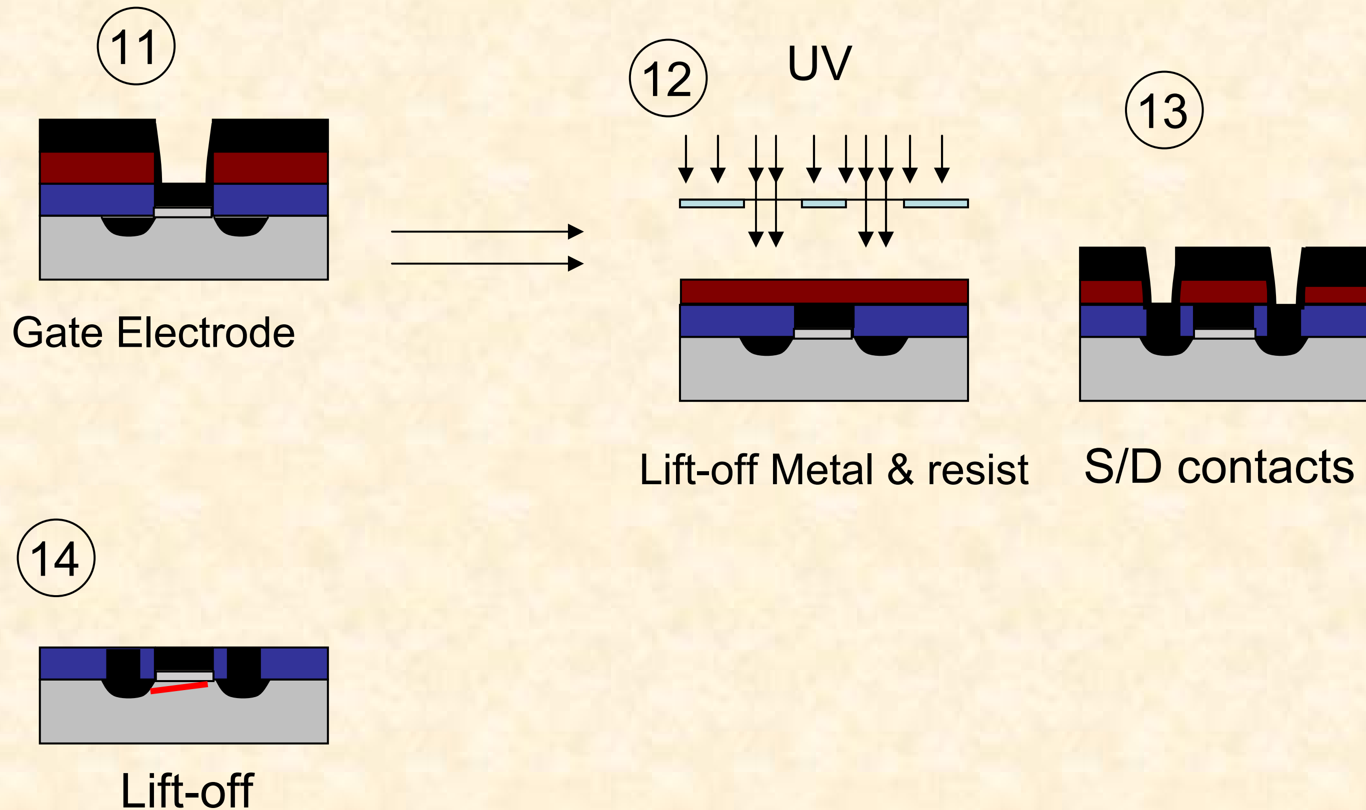
The steps are:

Wafer cleaning
Barrier layer formation
Photo-resist application
Soft baking
Mask alignment
Exposure and development
Hard-baking.

Typical Fabrication Steps of a typical MOSFET



Cont. Typical Fabrication Steps of a typical MOSFET



Gate Oxide Thickness is typically less than 1 nm
Channel length is typically less than 65 nm.

Where Do We Make Them?

Clean Room Standards

Class	maximum particles/ft³					ISO equivalent
	≥0.1 μm	≥0.2 μm	≥0.3 μm	≥0.5 μm	≥5 μm	
1	35	7	3	1		ISO 3
10	350	75	30	10		ISO 4
100		750	300	100		ISO 5
1,000				1,000	7	ISO 6
10,000				10,000	70	ISO 7
100,000				100,000	700	ISO 8

- Natural, “fresh” air: 1 million per cubic foot , 0.5 μm in diameter.
- Human being sheds *one billion* flakes of skin in a 24 hour period.
- Standing still human, 100,000 particles per minute.
- Walking around the room at only 3 km/h releases 5 million particles per minute.

Special clothes and shoes must be used for filtering

Ken Sutherland, Filtration & Separation Volume 45, Issue 4, May 2008, Pages 20-22

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HVP4

Protect Yourself And Those Around You

Under which circumstances is it required to store chemicals in ventilated cabinets according to the authorities?
According to §13 of the Employee Protection Committee's regulations on laboratory work with chemicals (AFS 1997:10), chemicals that produce fumes which are hazardous to your health are required to be stored in mechanically ventilated cabinets or storage areas.

Nanotechnology

Nanotechnology is the understanding and control of matter at dimensions of roughly 1 to 100 nanometers, where unique phenomena enable novel applications.

1 nanometer = 1×10^{-9} m

How can we see nanostructures?

- **Scanning Electron Microscopes (SEM)**
  (Field-Emision FE-SEM ➔ high resolution)

Resolution ?!

- **A scanning probe microscope?**
  Atomic Force Microscopes (AFM)
  Transmission Electron Microscopes (TEM)

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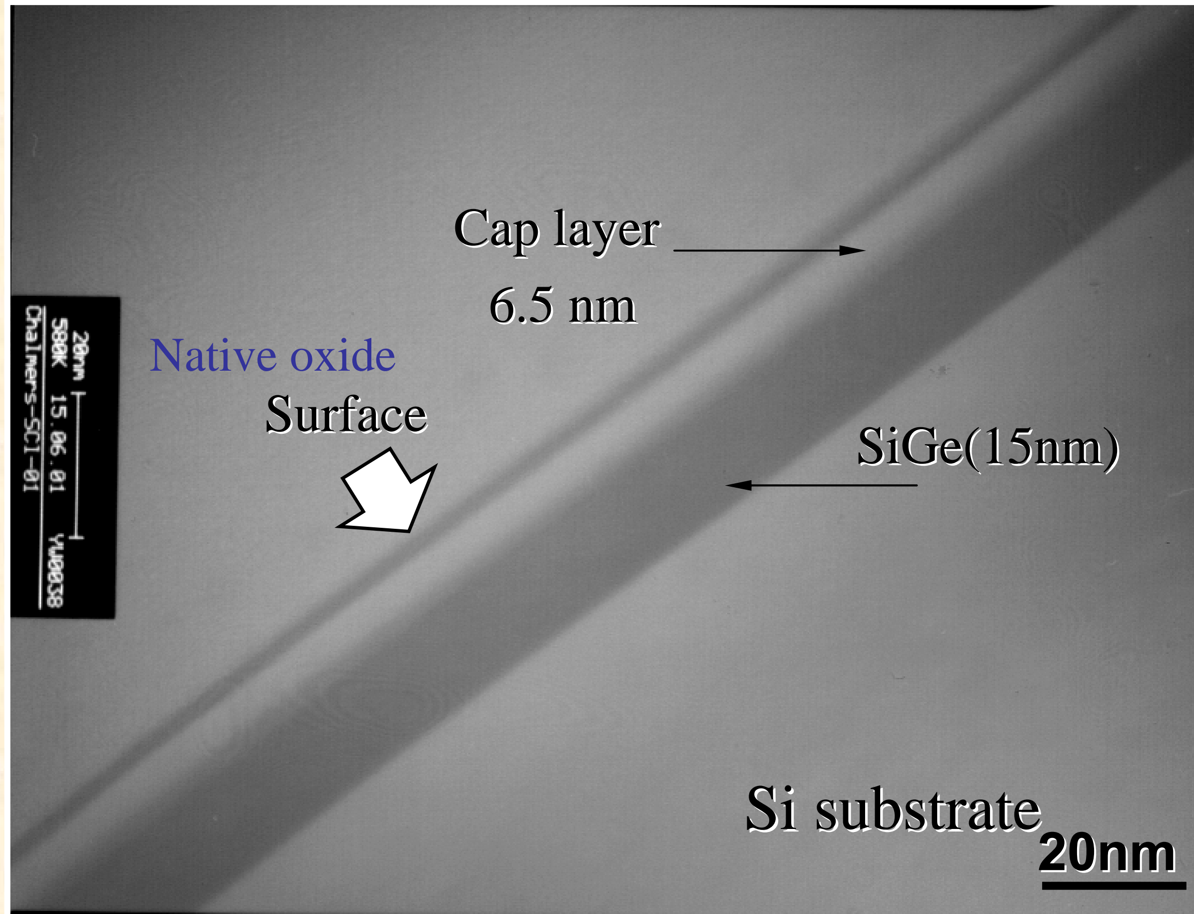
One SC1 Cycle. Etch~ 2.5 nm



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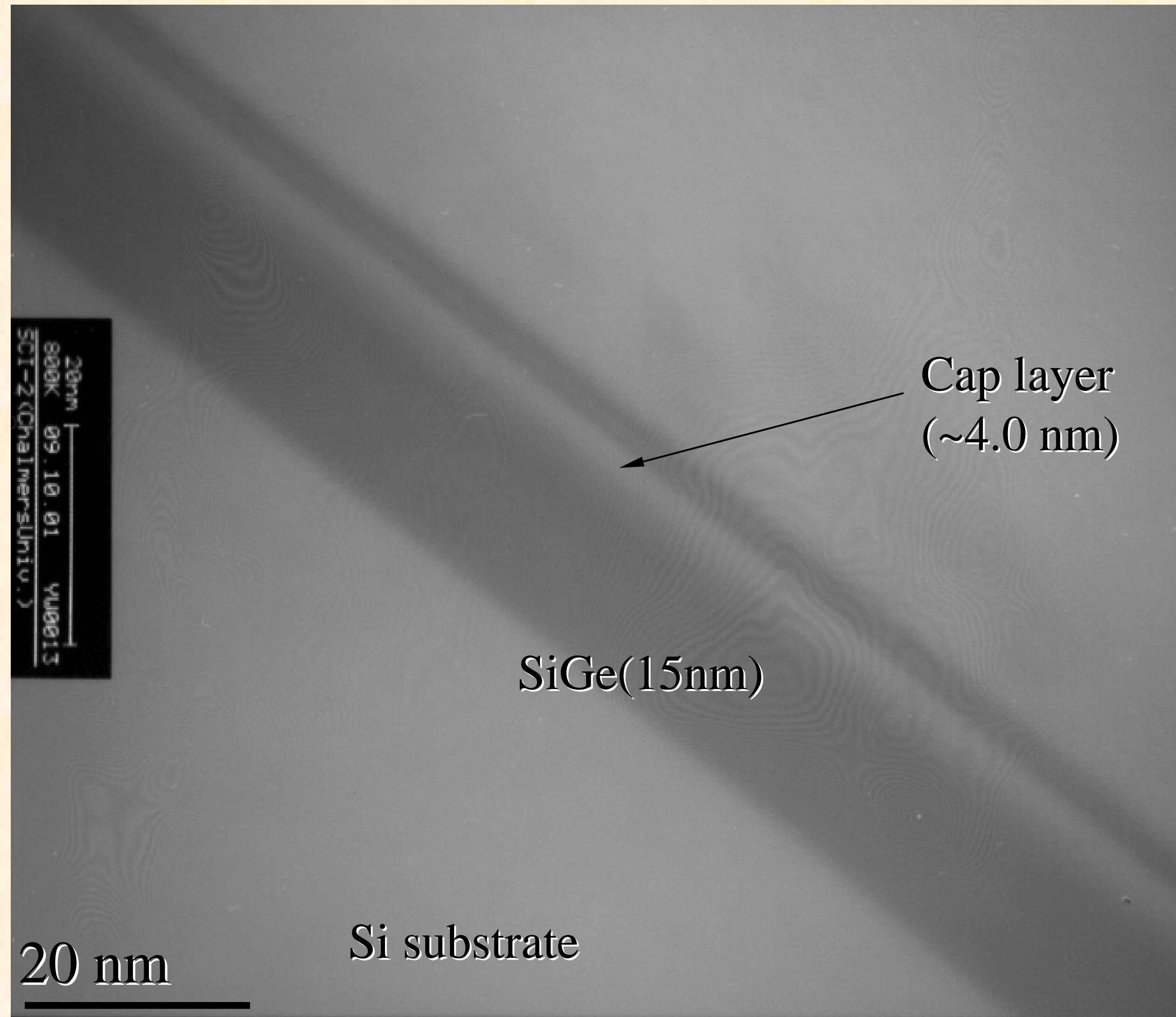

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Summary: The Impact of Nanotechnology on the MOSFET

- Brought the MOSFET to operate at frequencies in the GHz.

However

- At these GHz frequencies makes the power disspation by the devices to be the limiting factor for further conventional scaling.

➔ **This motivates extensive research for alternatives**

Emerging technologies would complement or replace the traditional Si MOSFET technology. These include (but not restricted to):

- Carbon Nanotube-based MOSFET
- Quantum Wire-based MOSFET
- Nanoelectromechanical Carbon Nanotube-based Switches for low power applications.